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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/436,984	11/09/1999	SHUNPEI YAMAZAKI	0756-2063	7375

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EXAMINER
COLEMAN, WILLIAM D

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 07/31/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/436,984	Applicant(s) YAMAZAKI ET AL.
	Examiner W. David Coleman	Art Unit 2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 July 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 32-55* is/are pending in the application.

4a) Of the above claim(s) *1-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *32-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *22, 23* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Claims 1-14 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected Invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in Paper No. 24.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 32-36, 38-41, 44-48 and 50-54 are rejected under 35 U.S.C. 102(b) as being anticipated by Hodate et al., U.S. Patent 5,518,940.

5. Hodate discloses a semiconductor devices as claimed. See **FIGS. 4A-4C, 5B** and **8A-8C**.

Pertaining to claim 32, Hodate teaches a semiconductor device comprising: (starting with

FIG. 8A-8C

a semiconductor film **43** formed on an insulating surface **42**; a channel forming region **44** in the semiconductor film; a gate insulating film **45** formed on the semiconductor film; a gate electrode **46** formed over the channel forming region **44** with the gate insulating film interposed therebetween; a pair of side walls **46** adjacent to side surfaces of the gate electrode **46**;

(now to **FIGS. 4A-4C**) a pair of first impurity regions **18** doped with an N-type impurity at a first concentration and formed in the semiconductor film with the channel forming region extending therebetween wherein the pair of side walls overlap the pair of first impurity regions; and a pair of second impurity regions **20** doped with an N-type impurity at a second concentration greater than the first concentration and formed in the semiconductor film adjacent to the pair of first impurity regions; and

a pair of third impurity regions **21** doped with an N-type impurity at a third concentration greater than the second concentration and formed in the semiconductor film with the pair of second impurity regions extending between the channel forming region and the pair of third impurity regions.

6. Pertaining to claim 33, Hodate teaches the semiconductor device according to claim 32 wherein the N-type impurity added in the first, second and third impurity regions comprises an element selected from the group 15 elements.

7. Pertaining to claim 34, Hodate teaches the semiconductor device according to claim 32 wherein the N-type impurity added in the first, second and third impurity regions comprises phosphorous (column 5, line 36).

8. Pertaining to claim 35, Hodate teaches the semiconductor device according to claim 32 wherein the side walls comprise silicon **4**.

9. Pertaining to claim 36, Hodate teaches the semiconductor device according to claim 32 wherein the semiconductor device is one selected from a liquid crystal display device, an EL display device and an image sensor (column 2, line 45).

10. Pertaining to claim 38, Hodate teaches a semiconductor device comprising: a semiconductor film formed on an insulating surface; a channel forming region in the semiconductor film;

a gate insulating film formed on the semiconductor film; a gate electrode formed over the channel forming region with the gate insulating film interposed therebetween;

a pair of conductive side walls adjacent to side surfaces of the gate electrode;

a pair of first impurity regions doped with an N-type impurity at a first concentration and formed in the semiconductor film with the channel forming region extending therebetween wherein the pair of side walls overlap the pair of first impurity regions; and

a pair of second impurity regions doped with an N-type impurity at a second concentration greater than the first concentration and formed in the semiconductor film adjacent to the pair of first impurity regions; and

a pair of third impurity regions doped with an N-type impurity at a third concentration greater than the second concentration and formed in the semiconductor film with the pair of second impurity regions extending between the channel forming region and the pair of third impurity regions.

11. Pertaining to claim 39, Hodate teaches the semiconductor device according to claim 38 wherein the N-type impurity added in the first, second and third impurity regions comprises an element selected from the group 15 elements.

12. Pertaining to claim 40, Hodate teaches the semiconductor device according to claim 38 wherein the N-type impurity added in the first, second and third impurity regions comprises phosphorous.

13. Pertaining to claim 41, Hodate teaches the semiconductor device according to claim 38 wherein the side walls comprise silicon.

14. Pertaining to claim 42, Hodate teaches the semiconductor device according to claim 38 wherein the semiconductor device is one selected from a liquid crystal display device, an EL display device and an image sensor.

15. Pertaining to claim 44, Hodate teaches a semiconductor device comprising:

(a) a thin film transistor over a substrate, said thin film transistor comprising: a semiconductor film formed on an insulating surface; a channel forming region in the semiconductor film; a gate insulating film formed on the semiconductor film; a gate electrode formed over the channel forming region with the gate insulating film interposed therebetween; a pair of side walls adjacent to side surfaces of the gate electrode; a pair of first impurity regions doped with an N-type impurity at a first concentration and formed in the semiconductor film with the channel forming region extending therebetween wherein the pair of side walls overlap the pair of first impurity regions; and a pair of second impurity regions doped with an N-type impurity at a second concentration greater than the first concentration and formed in the semiconductor film adjacent to the pair of first impurity regions; and a pair of third impurity

regions doped with an N-type impurity at a third concentration greater than the second concentration and formed in the semiconductor film with the pair of second impurity regions extending between the channel forming region and the pair of third impurity regions;

(b) an interlayer insulating film formed over the thin film transistor; and

See **FIG. 5C** for element (c) a pixel electrode **32p** formed over the interlayer insulating film **69** (as seen in **FIG. 10C**) and electrically connected to one of the third impurity regions.

16. Pertaining to claim 45, Hodate teaches the semiconductor device according to claim 44 wherein the N-type impurity added in the first, second and third impurity regions comprises an element selected from the group 15 elements.

17. Pertaining to claim 46, Hodate teaches the semiconductor device according to claim 44 wherein the N-type impurity added in the first, second and third impurity regions comprises phosphorous.

18. Pertaining to claim 47, Hodate teaches the semiconductor device according to claim 44 wherein the side walls comprise silicon.

19. Pertaining to claim 48, Hodate teaches the semiconductor device according to claim 44 wherein the semiconductor device is one selected from a liquid crystal display device, an EL display device and an image sensor.

20. Pertaining to claim 50, Hodate teaches a semiconductor device comprising:

(a) a thin film transistor formed over a substrate, said thin film transistor comprising: a semiconductor film formed on an insulating surface; a channel forming region in the semiconductor film; a gate insulating film formed on the semiconductor film; a gate electrode formed over the channel forming region with the gate insulating film interposed therebetween; a

pair of conductive side walls adjacent to side surfaces of the gate electrode; a pair of first impurity regions doped with an N-type impurity at a first concentration and formed in the semiconductor film with the channel forming region extending therebetween wherein the pair of side walls overlap the pair of first impurity regions; and a pair of second impurity regions doped with an N-type impurity at a second concentration greater than the first concentration and formed in the semiconductor film adjacent to the pair of first impurity regions; and a pair of third impurity regions doped with an N-type impurity at a third concentration greater than the second concentration and formed in the semiconductor film with the pair of second impurity regions extending between the channel forming region and the pair of third impurity regions;

(b) an interlayer insulating film formed over the thin film transistor; and

(c) a pixel electrode formed over the interlayer insulating film and electrically connected to one of the third impurity regions.

21. Pertaining to claim 51, Hodate teaches the semiconductor device according to claim 50 wherein the N-type impurity added in the first, second and third impurity regions comprises an element selected from the group 15 elements.

22. Pertaining to claim 52, Hodate teaches the semiconductor device according to claim 50 wherein the N-type impurity added in the first, second and third impurity regions comprises phosphorous.

23. Pertaining to claim 53, Hodate teaches the semiconductor device according to claim 50 wherein the side walls comprise silicon.

24. Pertaining to claim 54, Hodate teaches the semiconductor device according to claim 50 wherein the semiconductor device is one selected from a liquid crystal display device, an EL display device and an image sensor.

Claim Rejections - 35 USC § 103

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. Claims 37, 43, 49 and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hodate et al., U.S. Patent 5,518,940 as applied to claims 32-36, 38-42 and 44-54 above, and further in view of Shanks et al., U.S. Patent 5,821,688.

27. Hodate discloses a semiconductor device substantially as claimed as discussed above. However, Hodate fails to teach wherein the semiconductor device is one selected from a video camera, a digital camera, a projector, a goggle type display, a car navigation device, a personal computer and a portable information terminal. Shanks teaches a semiconductor device wherein it is one selected from a portable information terminal. See FIG. 1 of Shanks where a portable information terminal is disclosed. In view of Shanks, it would have been obvious to one of ordinary skill in the art to incorporate the portable information terminal of Shanks into the Hodate semiconductor device because it can be used in pilot interface applications (column 2, lines 36-37).

Double Patenting

28. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

29. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

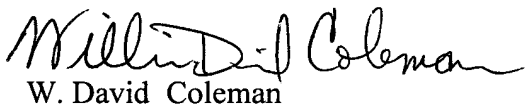
30. Claims 32, 35, 36, 37, 38, 41, 42, 43, 44, 47, 48, 49, 50, 53, 54 and 55 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 7, 8, 9, 15, 17, 19, 23, 25, 27, 37, 42, 44, 46, 57, 64, and 66 of U.S. Patent No. 6,274,887 B1. Although the conflicting claims are not identical, they are not patentably distinct from each other because it is well known in the art that a semiconductor thin film transistor includes an active layer.

Conclusion

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 703-305-0004. The examiner can normally be reached on 9:00 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7721 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



W. David Coleman
Examiner
Art Unit 2823

WDC
July 27, 2002